In the Claims:

- 1-14. (cancelled)
- 15. (amended) An integrated circuit comprising:
 - A. a semiconductor substrate;
- B. functional IP core circuits formed on the substrate, the IP core circuits forming a periphery on the substrate and having core functional input leads and core functional output leads that extend beyond that periphery; and
- C. test circuits formed on the substrate within the periphery of the functional IP core circuits, the test circuits including:
- i. a test data input lead extending beyond the periphery of the functional IP core circuits;
- ii. a test data output lead extending beyond
 the periphery of the functional IP core circuits;
- iii. a test clock lead extending beyond the periphery of the functional IP core circuits;
- iv. a test mode select lead extending beyond
 the periphery of the functional IP core circuits;
- v. a test access port coupled to the test data input lead, the test data output lead, the test clock lead, and the test mode select lead;
- vi. test data registers coupled to the test data input lead, and the test data output lead;
- vii. an instruction register coupled to the test data input lead and the test data output lead; and
- viii. an external register present lead <u>separate</u> from the test data input lead and the test data output lead, connected to the instruction register and extending beyond the periphery of the functional IP core circuits.

- 16. (previously presented) The integrated circuit of claim 15 in which the instruction register includes a capture-shift-update register section and the external register present lead is connected to the capture-shift-update register section.
- 17. (previously presented) The integrated circuit of claim 15 in which the instruction register includes a decode section and the external register present lead is connected to the decode section.
- 18. (previously presented) The integrated circuit of claim 15 in which the instruction register includes a capture-shift-update register section and a decode section and the external register present lead is connected to the capture-shift-update register section and the decode section.
- 19. (previously presented) The integrated circuit of claim 15 in which the external register present lead is only an input lead that carries only an input signal.